WHAT IS CLAIMED IS:

1. A synchronous SRAM-compatible memory having a DRAM array with a plurality of DRAM cells arranged in a matrix from defined by rows and columns, and interfacing with an external system for providing a row address and a column address, the DRAM cells requiring a refresh operation at selected intervals to maintain data stored therein, comprising:

a data input/output unit for controlling input and output of data to/from the DRAM array;

an address input unit for inputting a row address and a column address of a current frame in synchronization with an external clock signal when an effective address signal is activated;

a burst address generating unit for generating a burst address sequentially varying with respect to the column address in synchronization with the external clock signal;

a state control unit for generating a burst enable signal that enables the burst address generating unit, controlling the data input/output unit, and generating a wait indication signal of a first logic state while an access operation of a previous frame is performed with respect to the DRAM array, the access operation of the previous frame including a write access operation and a refresh operation before the effective address signal of the current frame is activated;

a refresh timer for generating a refresh request signal activated at selected intervals; and

a refresh control unit for controlling the refresh operation with respect to the DRAM array in response to the refresh request signal, the refresh operation being performed after completion of a burst access operation ongoing with respect to the DRAM memory array.

2. The synchronous SRAM-compatible memory as set forth in claim 1, wherein the wait indication signal has the first logic state while an operation of a column latency is performed.

3. The synchronous SRAM-compatible memory as set forth in claim 1, wherein the refresh control unit further comprises a refresh driving signal generating unit for activating a refresh driving signal for initiating the refresh operation with respect to the DRAM array in response to the refresh request signal, the activation of the refresh driving signal being suppressed by activation of a refresh masking signal.

4. The synchronous SRAM-compatible memory as set forth in claim 3, wherein the refresh control unit further comprises a refresh masking generating unit for generating the refresh masking signal, the refresh masking signal being enabled in

response to an effective address signal and being disabled in response to completion of the burst access operation.

5. The synchronous SRAM-compatible memory as set forth in claim 4, wherein the state control unit comprises:

an effective address signal detecting means for detecting activation end of the effective address signal; and

a burst termination detector for detecting termination of the burst access operation.

6. The synchronous SRAM-compatible memory as set forth in claim 1, wherein the data input/output unit receives and stores input data provided from an outside in synchronization with the external clock signal and writes the stored input data in the DRAM array, the writing of the stored input data being delayed till completion of the access operation of the previous frame while the access operation of the previous frame is performed.

7. The synchronous SRAM-compatible memory as set forth in claim 6, wherein the data input/output unit further comprises a First-In First-Out (FIFO) buffer for storing the received input data and writing the received input data in the DRAM array, the received input data being written in the DRAM array in a same order of reception.

8. A method of driving a synchronous SRAM-compatible memory having a DRAM array with a plurality of DRAM cells arranged in a matrix form defined by rows and columns, and interfacing with an external system for providing a row address and a column address, the DRAM cells requiring a refresh operation at selected intervals to maintain data stored therein, comprising:

(A) inputting an effective address signal, wherein the row and column addresses of a current frame are effectively input while the effective address signal is activated, and the row and column addresses of the current frame are not effectively input while the effective address signal is inactivated;

(B) determining whether an access operation of a previous frame is performed when activation of the effective address signal is detected;

(C) waiting for completion of the access operation of the previous frame and generating a wait indication signal of a first logic state to an outside when the access operation of the previous frame is determined to be performed in the step (B); and

(D) performing a burst access operation in which a burst address for selecting a column of the DRAM array is varied in synchronization with an external clock signal when the access

operation of the previous frame is determined to be completed in the step (B);

wherein the access operation of the previous frame includes a write access operation and a refresh operation generated before the effective address signal of the current frame is activated.

9. The method as set forth in claim 8, further comprising providing the wait indication signal of the first logic state while an operation of a column latency is performed.

10. The method as set forth in claim 8, further comprising performing the burst access operation when it is determined that the access operation of the previous frame is not performed in the step (B).

11. The method as set forth in claim 8, further comprising rendering the synchronous SRAM-compatible memory entered in an idle state when the burst access operation is completed.

12. The method as set forth in claim 8, further comprising:

activating a refresh request signal that requests a refresh operation with respect to the DRAM array at selected

intervals; and

performing the refresh operation after completion of the burst access operation when the refresh request signal is activated during the burst access operation.

13. The method as set forth in claim 8, further comprising:

receiving input data provided from an outside in synchronization with the external clock signal;

storing the received input data in an internally installed buffer; and

writing the received input data stored in the buffer in the DRAM array, the writing of the received input data being delayed till completion of an access operation of a previous frame while the access operation of the previous frame is performed.

14. The method as set forth in claim 13, wherein the writing of the received input data is performed in a same order of the storing of the received input data in the buffer.